CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (currently amended) A method for generating an FPGA bitstream having bits representing configuration of the FPGA and bits controlling loading of the bitstream, comprising:

generating an unencrypted bitstream including both the bits representing the configuration of the FPGA and the bits controlling loading of the bitstream; and

encrypting the bits representing the configuration of the FPGA using at least one key; and

combining the bits controlling loading of the bitstream with the encrypted bits representing the configuration of the FPGA to produce a partially encrypted bitstream;

wherein the at least one key is stored in volatile memory that may be powered by a battery; and

wherein the at least one key includes key order data indicating whether the at least one key is a first or only key.

2. (original) The method of Claim 1 further comprising:

loading the partially encrypted bitstream into the FPGA;

decrypting the partially encrypted bitstream within the FPGA using the key; and

configuring the FPGA using the decrypted bitstream.

3. (original) The method of Claim 2 wherein the key for decrypting the bits representing the configuration of the FPGA is stored in the FPGA.

4-5. (canceled)

6. (original) The method of Claim 1 wherein some bits controlling loading of the bitstream provide an indication that the bits representing configuration of the FPGA are encrypted.

7. (currently amended) A method for generating an FPGA bitstream having bits representing configuration of the FPGA and bits controlling loading of the bitstream, comprising:

providing an indication as to whether the bits representing configuration of the FPGA are to be encrypted;

generating an unencrypted bitstream including both the bits representing the configuration of the FPGA and the bits controlling loading of the bitstream; and

if the indication indicates that the bits representing configuration of the FPGA are to be encrypted, encrypting the bits representing the configuration of the FPGA;

wherein the encrypting comprises encrypting the bits representing configuration of the FPGA using at least one key stored in volatile memory of the FPGA that may be powered by a battery; and

wherein the at least one key includes key order data indicating whether the at least one key is a first or only key.

8. (previously presented) The method of claim 1, wherein the step of generating an unencrypted bitstream comprises including a key address in the bits that control loading of the bitstream, and the key address references an addressable storage element in the FPGA in which the at least one key is stored.

9. (previously presented) The method of claim 8, further comprising:

loading the partially encrypted bitstream into the FPGA;

reading the at least one key from the storage element referenced by the key address;

decrypting the partially encrypted bitstream within the FPGA using the at

least one key; and

configuring the FPGA using the decrypted bitstream.

10. (previously presented) The method of 9, further comprising storing in the FPGA a plurality of keys, and wherein the key address references one of the plurality of keys.

11. (currently amended) An apparatus for generating an FPGA bitstream having bits representing configuration of the FPGA and bits controlling loading of the bitstream, comprising:

means for generating an unencrypted bitstream including both the bits representing the configuration of the FPGA and the bits controlling loading of the bitstream; and

means for encrypting the bits representing the configuration of the FPGA using at least one key; and

means for combining the bits controlling loading of the bitstream with the encrypted bits representing the configuration of the FPGA to produce a partially encrypted bitstream;

wherein the at least one key is stored in volatile memory that may be powered by a battery; and

wherein the at least one key includes key order data indicating whether the at least one key is a first or only key.

12. (currently amended) An apparatus for generating an FPGA bitstream having bits representing configuration of the FPGA and bits controlling loading of the bitstream, comprising:

means for providing an indication as to whether the bits representing configuration of the FPGA are to be encrypted;

means for generating an unencrypted bitstream including both the bits representing the configuration of the FPGA and the bits controlling loading of the bitstream; and

means, responsive to the indication indicating that the bits representing configuration of the FPGA are to be encrypted, for encrypting the bits representing the configuration of the FPGA;

wherein at least one key stored in volatile memory of the FPGA that may be powered by a battery is used by the means for encrypting; and

wherein the at least one key includes key order data indicating whether the at least one key is a first or only key.